

PROGRAMMABLE STORAGE NETWORK PROTOCOL HANDLER ARCHITECTURE

Abstract of the Disclosure

An architecture that achieves high speed performance in a network protocol handler combines parallelism and pipelining in multiple programmable processors, along with specialized front-end logic at the network interface that handles time critical protocol operations. The multiple processors are interconnected via high-speed interconnect, and each processor's memory is globally accessible by other processors. Each processor has multiple threads, each capable of fully executing programs. Each processor contains embedded dynamic random access memory (DRAM). Threads within a processor are assigned the processing of various protocol functions in a parallel/pipelined fashion. Data frame processing is done by one or more of the threads to identify related frames. Related frames are dispatched to the same thread so as to minimize the overhead associated with memory accesses and general protocol processing. The high-speed protocol handler may also provide built-in monitors for examining the activity of its hardware resources and reallocating the workload to the resources that are not heavily used, thus balancing the resource utilization and increasing the workload throughput.

Figures

Figure 1: A diagram illustrating the structure of a document. It shows a vertical sequence of elements: a title, a list of figures, and a list of tables. The title is at the top, followed by the list of figures, and then the list of tables. The list of figures is a vertical sequence of figure numbers and titles. The list of tables is a vertical sequence of table numbers and titles. The diagram shows the relative positions of these elements in a document.